EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	180	(john with heck) or (joseph with s with hayden) or (steve with w with greathouse) or (daniel with m with wong)	US-PGPUB; USPAT	OR	ON	2007/02/27 17:29
L3	44	2 and MEMS	US-PGPUB; USPAT	OR	ON	2007/02/27 17:30
L4	16	3 and @ad<"20030630"	US-PGPUB; USPAT	OR	ON	2007/02/27 17:52
L5	5	cap and 4	US-PGPUB; USPAT	OR	ON	2007/02/27 17:35
L6	4229	MEMS and cap and @ad<"20030630"	US-PGPUB; USPAT	OR	ON	2007/02/27 17:39
L7	3457	6 and vias	US-PGPUB; USPAT	OR	ON	2007/02/27 17:37
L8	16	7 and (MEMS with dice)	US-PGPUB; USPAT	OR	ON	2007/02/27 17:37
L9	3258	MEMS and cap and via	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 17:40
L10	1	(MEMS with dice) and cap and via	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 17:40
L11	157	(MEMS same dicing) and @ad<"20030630"	US-PGPUB; USPAT	OR	ON	2007/02/27 18:13
L12	103	(MEMS same dicing) and via and @ad<"20030630"	US-PGPUB; USPAT	OR	ON	2007/02/27 18:13
L13	0	12 not 11	US-PGPUB; USPAT	OR	ON	2007/02/27 18:13
L14	13	(MEMS same dicing) and plug and @ad<"20030630"	US-PGPUB; USPAT	OR	ON	2007/02/27 18:14

US-PAT-NO: 6586831

DOCUMENT-IDENTIFIER: US 6586831 B2
See image for Certificate of Correction

TITLE: Vacuum package fabrication of integrated circuit components

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Application Filing Date - AD (1):
20010810

Brief Summary Text - BSTX (5):
Many **MEMS** devices require a vacuum environment in order to attain maximum performance. The vacuum package also provides protection and an optimal operating environment for the **MEMS** device. Examples of these **MEMS** devices are infrared **MEMS** such as bolometers and certain inertial **MEMS** such as gyros and accelerometers. Currently **MEMS** devices are individually packaged in vacuum compatible packages after fabrication and **dicing of the MEMS** device. Often, packaging costs of **MEMS** devices is 10 to 100 times the fabrication costs. These high packaging costs make it difficult to develop commercially viable vacuum packaged **MEMS** devices.

Brief Summary Text - BSTX (6):
MEMS devices are fragile especially after **dicing**. Care must be taken in handling these devices, and traditional integrated circuit fabrication machinery cannot adequately handle and protect **MEMS** devices. Therefore, special handling techniques have been developed to protect the **MEMS** devices until vacuum packaging has been completed. These special handling procedures add additional cost to the production of **MEMS** devices.

Brief Summary Text - BSTX (11):
The present invention provides various advantages over traditional vacuum packaging methods. One technical advantage of the present invention is that vacuum packaging is incorporated into the fabrication process of **MEMS** devices. Another technical advantage is the elimination of individual **MEMS** vacuum packaging and individual die handling. Yet another advantage of the present invention is that all **MEMS** devices on a silicon wafer are vacuum packaged at one time during device fabrication, thereby significantly reducing the costs

associated with vacuum packaging **MEMS** devices. This reduction in costs should result in the development of commercially viable **MEMS** devices. Yet another advantage of the present invention is that **MEMS** devices are protected at an earlier stage in fabrication. Another advantage is the ability to use traditional methods of handling integrated circuits after a **MEMS** device is vacuum packaged and diced. Still another advantage of the present invention is the ability to test all **MEMS** devices after vacuum packaging but before **dicing** using traditional integrated circuit testing procedures. Other advantages may be readily ascertainable by those skilled in the art.

Detailed Description Text - DETX (11):

Referring to FIG. 5, there is illustrated a silicon lid wafer 30. Although the preferred embodiment utilizes a silicon wafer as a substrate for the lid wafer 30, any suitable substrate material may be used. Lid wafer 30 includes a plurality of lid sealing rings 32 corresponding in number to device sealing rings 16 on device wafer 10. Each of the lid sealing rings 32 is a mirror image of a device sealing ring 16 so that lid wafer 30 mates with device wafer 10. Cavities 34 and bonding pad channels 36 are etched in the lid wafer 30 using an appropriate process such as wet or dry etching. The etching process for cavities 34 and bonding pad channels 36 may include depositing a layer of silicon nitride and patterning the silicon nitride layer to form an appropriate etch mask. An orientation dependent etch, or other suitable process, is then used to form cavities 34 and bonding pad channels 36. The silicon nitride layer may be removed before depositing the seal rings 32. Each of the cavities 34 is surrounded by a lid sealing ring 32. The function of the cavities 34 is to provide increased volume for a vacuum packaged **MEMS** device 12. As discussed below, the increased volume for the vacuum packaged **MEMS** device 12 provides for a higher vacuum level within the vacuum cell. Cavities 34 may be optional in some embodiments of the present invention that do not require a high vacuum. The function of the bonding pad channel 36 is to provide clearance over bonding pads 14 so that a **dicing** saw, etching process, or other suitable process may be used in a later step to open the lid wafer to expose the bonding pads for device testing before **dicing** of the wafer.

Detailed Description Text - DETX (30):

After testing the **MEMS** devices 12, the device wafer 10 is diced by sawing through probe channels 54 between bonding pads 14. In addition, a **dicing** saw is run between all vacuum package areas 52. The **dicing** of assembly 50 may be accomplished by using traditional methods of **dicing** silicon wafers with completed integrated circuits. By vacuum packaging **MEMS** devices 12 at the wafer level, traditional methods of handling integrated circuit devices may be used since the vacuum package provides protection to the delicate **MEMS** device

Detailed Description Text - DETX (40):

The method then proceeds to step 210 where the device wafer 10 is aligned with the lid wafer 30. After alignment, each device sealing ring 16 is aligned with its corresponding lid sealing ring 32. The method then proceeds to step 212 where the device wafer 10 is mated with the lid wafer 30 in a vacuum environment thus creating a plurality of vacuum packaged **MEMS** devices 12. The method then proceeds to step 214 where each vacuum packaged **MEMS** device 12 is tested using traditional integrated circuit testing procedures. In order to facilitate testing, probe access channels are opened above bonding pads 14 coupled to vacuum packaged **MEMS** devices 12. The method then proceeds to step 216 where the completed assembly 50 is diced using traditional integrated circuit **dicing** techniques.